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PTO/SB/08A (08-03)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/710861
		Filing Date	August 9, 2004
		First Named Inventor	Anindya Saha, et al.
		Group Art Unit	2816
		Examiner Name	
Sheet 1 of	Attorney Docket No.	TI-36220	

U.S. PATENT DOCUMENTS						
Exam. Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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/KA/	BA	JP	10322019a		NEC Nigata Ltd	5/21/97	Abstract	
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Examiner Signature	/Khareem Almo/	Date Considered	09/27/2007
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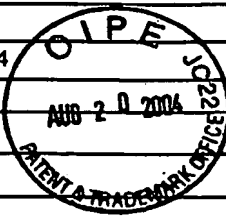
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Application Number	10/710,861	
			Filing Date	August 09, 2004	
			First Named Inventor	Anindya SAHA	
			Group Art Unit	UNASSIGNED	
			Examiner Name	UNASSIGNED	
Sheet	2	of	2	Attorney Docket Number	TI-36220



OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
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/KA/		PETER MACKEN, MARC DEGRAUWE, MARK VAN PAEMEL, HENRI OGUEY, "A Voltage Reduction Technique for Digital Systems" in ISSCC 90/ Session 15. Innovative Circuit design, Swiss Center for Electronics and Microtechnology (CSEM) Neuchel Switzerland/ FPM 15.2, pp.238 - 239/ Friday, February 16, 1990	
/KA/		THOMAS D. BURD AND ROBERT W BRODERSEN, "Design Issues for Dynamic Voltage Scaling", ISLPED '00 Rapallo, Italy, Berkeley Wireless Research center, University of California, CA/ pp.09 - 14, ACM, 2000	
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/KA/		KEVIN J. NOWKA, GARY D. CARPENTER, ERIC W. MAC DONALD, HUNG C. NGO, BISHOP C. BROCK, KOJI I. ISHII, TUYET Y. NGUYEN AND JEFFREY L. BURNS. "A 32-bit PowerPC System-on-a-Chip with support for Dynamic Voltage Scaling and Dynamic Frequency Scaling", in IEEE Journal of Solid State Circuits Vol.37, pp.1441 - 1447, NO.11 November 2002.	
/KA/		REX MIN, TRAVIS FURRER AND ANANTHA CHANDRAKASAN, "Dynamic Voltage Scaling Techniques for Distributed Microsensor Networks", Department of EECS, Massachusetts Institute of Technology. 2002	
/KA/		MOHAMED ELGEBALY, AMR FAHIM, INYUP KANG AND MANOJ SACHDEV, "Robust and Efficient Dynamic Voltage Scaling Architecture" Department of Electrical and Computer Engineering, University of Waterloo, Ontario, N2L 3G1 Canada, Qualcomm Inc, San Diego, CA, 92121 USA. IN IEEE, PP. 155- 158, 2003.	
/KA/		A.SOTO, A DE CASTRO, P. ALOU, J.A. CAO BOS, J. UCEDA AND A. LOTFI. "Analysis of the Buck Converter for Scaling the Supply Voltage of Digital Circuits". Universidad Politécnica de Madrid (UPM), Spain and Enpirion Inc, USA, IN IEEE, PP. 711 - 717, 2003	

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